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Description

METHOD FOR FABRICATING A TRENCH HAVING A BURIED DIELECTRIC COLLAR

BACKGROUND OF INVENTION

[0001] The present invention relates to the field of semiconductor device fabrication; more specifically, it relates to a method fabricating a trench and a trench capacitor having buried dielectric collars.

[0002] One use for trench capacitors is for the storage node of dynamic random access memory (DRAM) cells. In such applications there are parasitic sidewall leakage currents from a bitline of the DRAM cell to the storage node and from the storage node to the substrate. Buried dielectric collars are used to reduce these leakages. However, present schemes for forming buried collars are limited in the width of the collar formed (and thus limit leakage reduction) and are difficult to scale as trench widths decrease. Therefore, there is a need for a scalable buried dielectric collar process and reduced leakage trench capaci-

tor using a buried dielectric collar.

Summary of Invention

[0003] A first aspect of the present invention is a method of forming a buried dielectric collar around a trench, comprising: (a) forming the trench in a substrate; (b) forming a multilayer coating on sidewalls and a bottom of the trench; (c) removing a continuous band of the multilayer coating from the sidewalls a fixed distance from a top of the trench to expose a continuous band of substrate in the sidewalls of the trench; (d) etching, in the exposed band of substrate, a lateral trench extending into the substrate in the sidewalls of the trench; and (e) filling the lateral trench with a dielectric material to form the buried dielectric collar.

[0004] A second aspect of the present invention is a method of forming a trench capacitor, comprising: (a) forming a trench in a substrate; (b) forming a multilayer coating on sidewalls and a bottom of the trench; (c) removing a continuous band of the multilayer coating from the sidewalls a fixed distance from a top of the trench to expose a continuous band of substrate in the sidewalls of the trench; (d) etching, in the exposed band of substrate, a lateral trench extending into the substrate in the sidewalls of the

trench; (e) filling the lateral trench with a dielectric material to form the buried dielectric collar; (f) filling the trench with polysilicon.

[0005] A third aspect of the present invention is a method of forming a buried dielectric collar around a trench, comprising: (a) forming the trench in silicon substrate; (b) forming a multilayer coating on sidewalls and a bottom of the trench, the multilayer coating comprises in order from the substrate outward, a layer of silicon oxide, a first layer of silicon nitride, a layer of polysilicon and a second layer of silicon nitride; (c) forming a first resist fill a first distance from a top of the trench; (e) removing the first silicon nitride layer not protected by the first resist fill exposing a upper portion of the polysilicon layer and oxidizing an outer layer of the upper portion of the polysilicon layer to form a second silicon oxide layer on the polysilicon layer and then removing the first resist fill; (f) forming a second resist fill a second distance from a top of the trench, the second distance being greater than the first distance; (g) removing in the order recited, (i) between the second silicon oxide layer and a top surface of the second fill resist, a continuous band of the second silicon nitride layer, a continuous band of the polysilicon layer, a contin-

uous band of the first silicon nitride layer and a continuous band of the first silicon oxide layer to expose a continuous band of substrate in the sidewalls of the trench and the second resist fill or (ii) between the second silicon oxide layer and a top surface of the second fill resist, a continuous band of the second silicon nitride layer, a continuous band of the polysilicon layer and a continuous band of the first silicon nitride layer and then removing the second fill resist and the first silicon oxide layer to expose a continuous band of substrate in the sidewalls of the trench; (h) etching, in the exposed band of substrate, a lateral trench extending into the substrate in the sidewalls of the trench; and (i) filling the lateral trench with a dielectric material to form the buried dielectric collar.

Brief Description of Drawings

[0006] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0007] FIGs. 1 through 11 are partial cross-sectional views illustrating fabrication of a trench having a buried dielectric collar according to the present invention; and

[0008] FIGs. 12 through 15 are partial cross-sectional views illustrating further fabrication steps for forming a bottle trench capacitor according to the present invention.

Detailed Description

[0009] FIGs. 1 through 11 are partial cross-sectional views illustrating fabrication of a trench having a buried dielectric collar according to the present invention. In FIG. 1, formed in a substrate 100 is a trench 105. Substrate 100 may be a bulk silicon substrate or a silicon-on-insulator (SOI) substrate. Substrate 100 may include an uppermost epitaxial silicon layer. For the purposes of the present invention, a silicon substrate is defined as a bulk silicon substrate, the silicon layer of a SOI substrate, an uppermost epitaxial silicon layer formed on either a bulk or SOI substrate or a silicon layer formed on a substrate of any other material. Trench 105 may be formed by any number of anistropic etch processes, such as plasma etching and reactive ion etching (RIE), known in the art using a hard mask that is lithographically defined. A top surface 110 of substrate 100 defines a horizontal or lateral direction and a vertical direction is defined as a direction perpendicular to the horizontal direction. Trench 105 includes sidewalls 115 and a bottom 120. Formed on top surface 110 of

substrate 100, sidewalls 115 and bottom 120 of trench 105 is a silicon oxide layer 125. Formed over silicon oxide layer 125, including over those portions of the silicon oxide layer formed in trench 105, is a first silicon nitride layer 130. Formed over first silicon nitride layer 130, including over those portions of the first silicon nitride layer formed in trench 105, is a polysilicon layer 135. Formed over polysilicon layer 135, including over those portions of the polysilicon layer formed in trench 105, is a second silicon nitride layer 140.

[0010] Silicon oxide layer 125 may be formed by thermal oxidation of substrate 100 after trench 105 has been formed and the hard mask used to define the trench removed. Alternatively, the hard mask may be incorporated into that portion of silicon oxide layer 125 contacting top surface 110 of substrate 100. First silicon nitride layer 130, polysilicon layer 135 and second silicon nitride layer 140 are conformal coatings and may be formed by any number of methods, such as chemical-vapor deposition (CVD), low pressure chemical-vapor deposition (LPCVD) and plasma enhanced chemical-vapor deposition (PECVD) known in the art.

[0011] In one example, silicon oxide layer 125 is about 20 to 50

Å thick, first silicon nitride layer 130 is about 80 Å or greater thick, polysilicon layer 135 is about 200 Å or less thick and second silicon nitride layer 140 is about 40 to 80 Å thick.

[0012] In FIG. 2, a layer of resist 145 is formed on second silicon nitride layer 140 and completely fills trench 105. In FIG. 3, resist layer 145 is recessed to a depth D1 measured from top surface 110 of silicon substrate 100. Depth D1 defines an upper region 150 of trench 105. Depth D1 may be selected to correspond to the bottom of a P-well formed in an upper region of substrate 100 in which an NFET of a DRAM memory cell will be formed. In one example D1 is about 0.6 to 1.0 microns. In FIG. 4, a portion of second silicon nitride layer 140, not protected by resist layer 145 is removed, for example, by chemical downstream etch (CDE) or other plasma based etching process, thus exposing polysilicon layer 135 in upper region 150 of trench 105. In FIG. 5, resist layer 145 (see FIG. 4) is removed, for example, by a plasma strip process and exposed surfaces (those not covered by second silicon nitride layer 140) of polysilicon layer 135 are thermally oxidized to form a silicon oxide layer 155. About half of the thickness of polysilicon layer 135 is converted to oxide in

upper region 150 of trench 105 over top surface 110 of silicon substrate 100.

[0013] In FIG. 6, layer of resist 160 is formed on silicon oxide layer 155 and on remaining second silicon nitride layer 140 in trench 105. Resist layer 160 completely fills trench 105. In FIG. 7, resist layer 160 is recessed to a depth D2 measured from top surface 110 of silicon substrate 100. The difference D3 between depths D1 and D2 defines middle region 165 of trench 105. Depth D2 may be selected to correspond to the top of an N+ buried diffused plate often used to isolate DRAM memory cells. In one example D2 is about 1.3 to 1.7 microns.

[0014] In FIG. 8, a portion of second silicon nitride layer 140, not protected by resist 160 is removed, for example, by a CDE or other plasma based etching process selective silicon nitride to silicon oxide, thus exposing polysilicon layer 135 in middle region 165 of trench 105. Next, exposed polysilicon layer 135 in middle region 165 of trench 105 is removed, for example, by a CDE or other plasma based etching process selective silicon to silicon oxide, thus exposing first silicon nitride layer 130 in middle region 165 of trench 105. Next, exposed first silicon nitride layer 130 in middle region 165 of trench 105 is removed, for exam-

ple, by a CDE or other plasma based etching process selective silicon nitride to silicon oxide, thus exposing silicon oxide layer 125 in middle region 165 of trench 105.

[0015] In FIG. 9, resist 160 (see FIG. 8) is removed by, for example, by a plasma strip process and the exposed region of silicon oxide layer 125 in middle region 165 of trench 105 is removed using, for example using a 40:1 (HF to water) BHF etch. Silicon oxide layer 125 may also be removed using a dry etch. A small amount of silicon oxide layer 155 is also removed, but some of silicon oxide layer 155 remains because silicon oxide layer 155 is thicker than silicon oxide layer 125. Alternatively, resist layer 160 (see FIG. 8) may be removed after the removal of silicon oxide layer 125 in middle region 165 of trench 105. In either case, sidewall 115 of trench 105 in middle region 165 of the trench is exposed. The region of removed silicon oxide layer 125, removed first silicon nitride layer 130, removed polysilicon layer 135 and removed second silicon nitride layer 140 extends in a continuous band on all sidewalls of trench 105 and the vertical extent of which is defined by middle region 165 where a buried collar will be formed as described infra.

[0016] In FIG. 10, a lateral trench 170 is etched into sidewalls

115 in middle region 165 of trench 105 a distance D4. In one example, D4 may be selected to give, after the process illustrated in FIG. 11 and described infra, a filled lateral trench wide enough (in the horizontal direction to reduce parasitic leakages associated with subsequent structures, such as a trench capacitor. In a second example D4 may be selected to allow filled lateral trenches 170 of adjacent trenches 105 to contact one another after filling the lateral trenches with dielectric material using the process illustrated in FIG. 11 and described infra. At the same time silicon substrate 100 is etched, by a CDE or other plasma based etching process selective silicon to silicon oxide, to form lateral trenches 170 polysilicon layer 130 is also etched forming voids 175A between first silicon nitride layer 130 and silicon oxide layer 155. Voids 175B between first silicon nitride layer 130 and second silicon nitride layer 140 are formed simultaneously with voids 175A.

[0017] In FIG. 11, a thermal local oxidation of silicon (LOCOS) process is performed to oxidize all exposed silicon surfaces and fill lateral trenches 170 with silicon oxide forming buried dielectric collar 180. Buried dielectric collar 180 extends outward (and inward to a lesser degree) on all sidewalls of trench 105, and is continuous thus form-

ing a ring or collar. If trench 105 is circular, then buried dielectric collar 180 has the form of an annular ring. The thermal oxidation results in an increase in volume of the consumed silicon; the oxide thus formed being about 60% into the silicon substrate and about 40% exterior to the silicon substrate. It is this 40% that fills lateral trench 170. Thus, buried dielectric collar 180 extends a distance D5 (where D5>D4, see FIG. 10) into silicon substrate 100 from sidewalls 115, a distance D6 into trench 105 from sidewalls 115 and extends above and below lateral trench 170 in silicon substrate 100 a distance D7 due to conversion of silicon to silicon oxide. Consequentially, upper region 150 of FIG. 10 has shrunk in vertical extent to form upper region 150A of FIG. 11 and middle region 165 of FIG. 10 has expanded in vertical extent to form middle region 165A of FIG. 11. In one example, D5 is about 125 nm. There is also oxidation of exposed polysilicon layer 140 to form silicon oxide plugs 185.

[0018] At this point fabrication of a lateral trench having a buried dielectric collar is completed. Continuing fabrication steps will be directed to forming a trench capacitor starting with the structure illustrated in FIG. 11. There are many alternative process schemes possible from this point onward

in the formation of a trench capacitor. For example, in the structure illustrated in FIG. 11, the polysilicon layer and the dielectric layers in the trench may be removed and new dielectric layers formed on the sidewalls and bottom of the trench, then the trench filled with doped polysilicon and CMP process performed to remove excess doped polysilicon from the surface of the substrate. Therefore, the fabrication steps illustrated in FIGs. 12 through 15 should be considered exemplary.

[0019] FIGs. 12 through 15 are partial cross-sectional views illustrating further fabrication steps for forming a bottle trench capacitor according to the present invention. In FIG. 12, a conformal third layer of silicon nitride 190 followed by a conformal layer of oxide 195 are deposited over exposed surfaces of first silicon nitride layer 130, polysilicon layer 135, second silicon nitride layer 140, silicon oxide layer 155 and buried dielectric collar 180. Third silicon nitride layer 190 protects silicon oxide layer 155 in region 150A of trench 105 from subsequent etch steps. Oxide layer 195 protects exposed first silicon nitride layer 130 in lateral trenches from subsequent etch processes. In one example third silicon nitride layer 190 is less than about 40 Åthick and oxide layer 195 is greater than about

100 Å. In one example oxide layer 195 is tetraethoxysilane (TEOS) oxide.

[0020] In FIG. 13, oxide layer 195 is etched, by a CDE or other plasma based etching process selective silicon oxide to silicon nitride, to remove oxide layer 195 of all surfaces except those in lateral trenches 170.

[0021] In FIG. 14, all exposed third silicon nitride layer 190 as well as portions of second silicon nitride layer 140, polysilicon layer 135, and first silicon nitride layer 130 over bottom 120 of trench 105 are removed by a one or more CDE or other plasma based etching processes selective silicon nitride/polysilicon to silicon oxide. Silicon oxide layer 125 over bottom 120 of trench 105 is removed using, for example using a 40:1 (HF to water) BHF etch. Silicon oxide layer 125 may also be removed using a dry etch.

[0022] In FIG. 15, a cavity 200 is isotropically etched into substrate 100 using a CDE or other plasma based etching process selective silicon to silicon oxide. A dielectric layer 205 is formed on the sidewalls of cavity 200 and then trench 105 and cavity 200 are filled with polysilicon 210 and a CMP process performed to planarize substrate 100 to form a buried dielectric collared trench capacitor 215.

The CMP process may also remove silicon oxide layer 155 and second silicon nitride layer 135 over top surface 110 of substrate 100. Alternatively all or some of the dielectric layers in trench 105 may be removed and/or new dielectric layers formed on the sidewalls and bottom of the trench, then the trench filled with polysilicon and CMP process performed to planarize the surface of the substrate. In the case that trench capacitor is used in a DRAM cell, Pwell region 220 and N+ plate region 225 are illustrated in approximate positions relative to buried dielectric collar 180.

[0023] Thus, the present invention provides a scalable buried dielectric collar process and reduced leakage trench capacitor using a buried dielectric collar.

[0024] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall

within the true spirit and scope of the invention.